

WHAT IS CLAIMED IS:

1           1. A method for fabricating a non-volatile memory device, the  
2           method comprising:  
3            providing a substrate;  
4            forming an oxide layer overlying the substrate;  
5            forming a buffer layer overlying the oxide layer;  
6            forming a ferroelectric material overlying the substrate;  
7            forming a gate layer overlying the ferroelectric material, the gate layer  
8            overlying a channel region; and  
9            forming a first source/drain region adjacent to a first side of the channel  
10          region and a second source/drain region adjacent to a second side of the channel region.

1           2. The method of claim 1 wherein the channel region is about 1  
2          micron and less.

1           3. The method of claim 1 wherein the ferroelectric material is a PZT  
2          bearing compound.

1           4. The method of claim 1 wherein the buffer layer is a magnesium  
2          bearing compound.

1           5. The method of claim 1 wherein the buffer layer is a magnesium  
2          oxide layer, the magnesium oxide layer being a barrier layer.

1           6. The method of claim 1 wherein the ferroelectric material has a  
2          thickness of less than about 1,000 Angstroms.

1           7. The method of claim 1 wherein the buffer layer has a thickness  
2          ranging from about 7 to 100 nanometers.

1           8. The method of claim 1 wherein the ferroelectric material has a  
2          thickness of about 100 Angstroms and greater.

1           9. The method of claim 1 wherein the ferroelectric material is PZT.

1           10. The method of claim 1 wherein the buffer layer is a barrier  
2          diffusion layer, the barrier diffusion layer substantially preventing diffusion between the  
3          ferroelectric material to the substrate.

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11. The method of claim 1 wherein the buffer material is sputtered  
from a substantially pure magnesium target to form a magnesium oxide layer.

12. The method of claim 11 wherein the sputtering is maintained at a  
temperature greater than about 400 degrees Celsius or greater than about 500 degrees  
Celsius.

13. The method of claim 1 wherein the buffer layer is thermally  
annealed.

14. The method of claim 1 wherein the ferroelectric material is highly  
oriented.

15. The method of claim 14 wherein the highly oriented material is a  
polycrystalline film.

16. The method of claim 1 wherein the ferroelectric film is  
substantially free from an amorphous structure.

17. The method of claim 15 wherein the polycrystalline film has a  
crystal structure of 100 angstroms and greater.

18. The method of claim 1 wherein buffer layer is a template to  
provide an oriented growth of the ferroelectric film.

19. The method of claim 1 wherein the oxide is provided by a dry  
oxidation process comprising an oxygen bearing compound.

20. The method of claim 1 wherein the oxide passivates the surface of  
the substrate to protect the channel region.

21. A method for fabricating a non-volatile memory device, the  
method comprising:  
3 providing a substrate;  
4 forming a first buffer layer overlying the substrate;  
5 forming a second buffer layer overlying the first buffer layer;  
6 forming a ferroelectric material overlying the substrate;

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forming a gate layer overlying the ferroelectric material, the gate layer  
8 overlying a channel region; and  
9 forming first and second doped regions adjacent to first and second ends of  
10 the channel region.

1 22. The method of claim 21, wherein the first buffer layer is a gate  
2 oxide layer, and the second buffer layer is a MgO layer.

1 23. The method of claim 21, wherein the first buffer layer is an  
2 amorphous layer, and the second buffer layer is a highly-oriented layer.

1 24. The method of claim 23, wherein the second buffer layer has a  
2 thickness of no more than 10 nm.

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1 25. A memory structure for integrated circuit devices, the structure  
2 comprising:  
3 a substrate;  
4 an oxide layer overlying the substrate;  
5 a buffer layer overlying the oxide layer;  
6 a ferroelectric material overlying the substrate;  
7 a gate layer overlying the ferroelectric material, the gate layer overlying a  
8 channel region; and  
9 a first source/drain region adjacent to a first side of the channel region and  
10 a second source/drain region adjacent to a second side of the channel region.

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